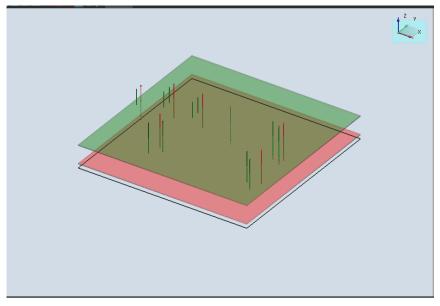
# Reducing Power and Ground Voltage Noise using Cadence PowerSI

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  - c. Finding Spatial distribution of voltage between power and ground plane
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  - a. Finding power/ground plane impedance Z11 at device locations
  - b. Placing decoupling capacitors to reduce resonant peak power/ground plane impedance

# I. Project Objective\*

In this project you will use PowerSI to determine value and locations of decoupling capacitors (maximum of 5) to reduce the power and ground voltage noise and impedance for a 5 layer printed circuit board.



Stackup	ackup Pad Stack									
Layer #	Color	Layer Icon	Layer Name	Thickness (mm)	Material	Conductivity (S/m)	Fill-in Dielectric	Frequency (Hz)	Er	Loss Tangent
1			Signal02	0.03556		5.800000e+07	[AIR]	1e+09	[1]	[0]
			Medium03	0.5		0			4	0
2			Plane02	0.03556		5.800000e+07	[FillPlane02_Average	1e+09	[4]	[0]
			Medium04	0.5		0			4	0
3			Signal03	0.03556		5.800000e+07	[FillSignal03_Avera	1e+09	[4]	[0]
			Medium02	0.1		0			4	0
4			Plane01	0.03556		5.800000e+07	[FillPlane01_Average	1e+09	[4]	[0]
			Medium01	0.1		0			4	0
5			Signal01	0.03556		5.800000e+07	[AIR]	1e+09	[1]	[0]

\*Note: In this tutorial:

- the dielectric constant is  $\varepsilon_r$ =4,
- the metal layers have thickness = 0.03556mm
- the dielectric layer thicknesses are
  - Layer 1: 0.5 mm.
  - Layer 2: 0.5 mm
  - Layer 3: 0.1 mm
  - Layer 4: 0.1 mm
- the plane x-y size is
  - x = 100 mm
  - y = 100 mm

\* These values may be different in your design

#### II. What is Cadence PowerSI

- PowerSI is a new generation power and signal integrity tool designed for the electrical analysis of integrated circuit packages and printed circuit boards.
- It provides fast and accurate full-wave results and allows designers to overcome the challenge of high-speed design issues related to power, ground, and signal integrity.
- PowerSI simulates electromagnetic field phenomenon by **full-wave methods** (e,g. direct solution of Maxwell's equations without approximations) in the frequency domain.
- PowerSI is used for the analysis and design of electronic packages including chip carriers and printed circuit boards.
- Package designers often analyze the power-ground system of a package by looking at its frequency-dependent impedance; the lower the impedance, the better the power and ground system.
- PowerSI Install instructions can be found at

https://docs.google.com/document/d/19mCAR2YfwvplPLo1\_ipDft8VabcYndrY3BfVrZvxIhM/edit?usp=sharing

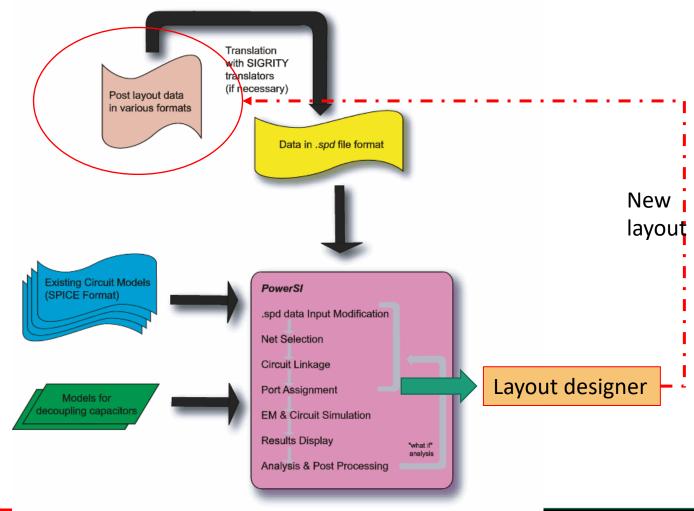
#### III. PowerSI Modes-Extraction

#### **Extraction Mode**

- Extraction Mode allows the easy and convenient extraction of S, Z, and Y parameters of multiple port networks that model package and board structures, such as the power delivery system.
- It can extract N-ports (of S, Z, and Y parameters) into the industry standard, Touchstone format, that can be used for subsequent analysis of larger scale systems.
- Combined with Sigrity Broadband SPICE, Extraction Mode provides highly accurate SPICE models over broadband frequencies, which can be used for transient analysis of modeled structures along with any active or passive circuits with commercial SPICE engines.

#### III. PowerSI Modes-Extraction Mode Flow

#### **PowerSI Extraction Mode Flow**

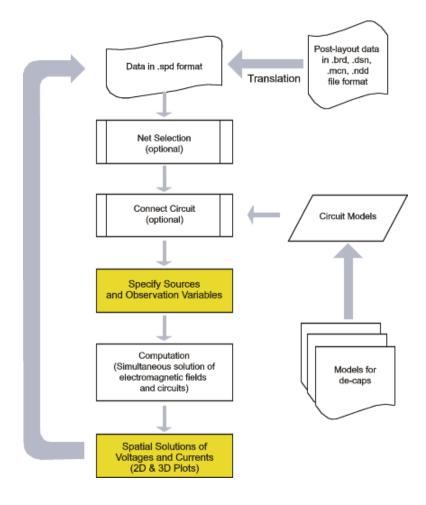


## III. PowerSI Modes-Spatial

#### **Spatial Mode**

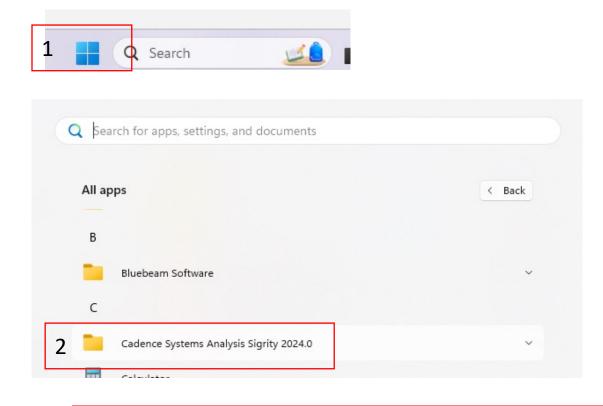
- Spatial Mode handles circuits containing multiple sources, and performs AC analysis on these circuits. It can obtain spatial variations of voltages across planes as well as voltages and currents in the circuit and physical structure components. Spatial Mode can also:
- Allow for multiple sources to be placed at various physical locations.
- Provides for easy and convenient assessment of spatial voltage distributions across the entire structure.
- Enable quick identification of "hot spots" and their corresponding frequencies where peak values occur.
- Determine the desired characteristics of decoupling capacitors at the most appropriate locations.

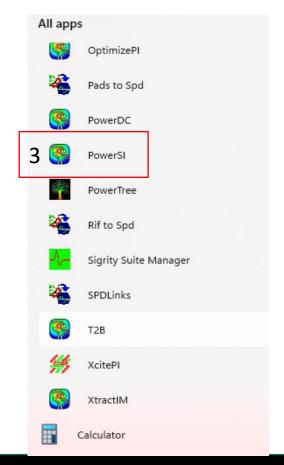
# III. PowerSI Modes-Spatial Mode Flow



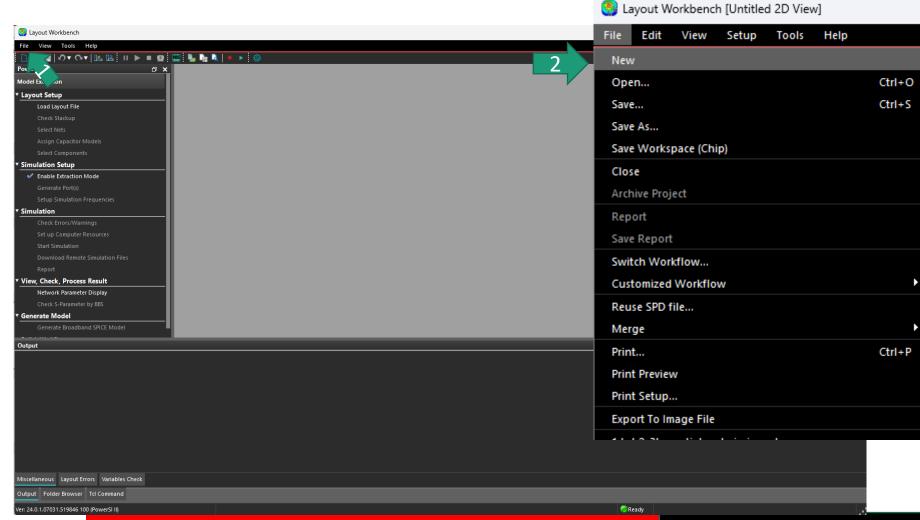
- Launch PowerSI
- 2. Start a New File; PCB model has by default number of layers is 4, size 100mm x 100mm
- 3. Edit the default stackup by adding a new signal layer between Plane01 and Plane02
- 4. Define a power (VDD) and a ground net (GND) and assign to Plane01 and Plane02
- 5. Check grid settings
- 6. Create new Pad Stack
- 7. Place VDD and GND vias for noise analysis

- 1. Go to all apps in Windows Start button
- 2. open Cadence Systems Analysis Sigrity 2024.0
- Double click PowerSI icon

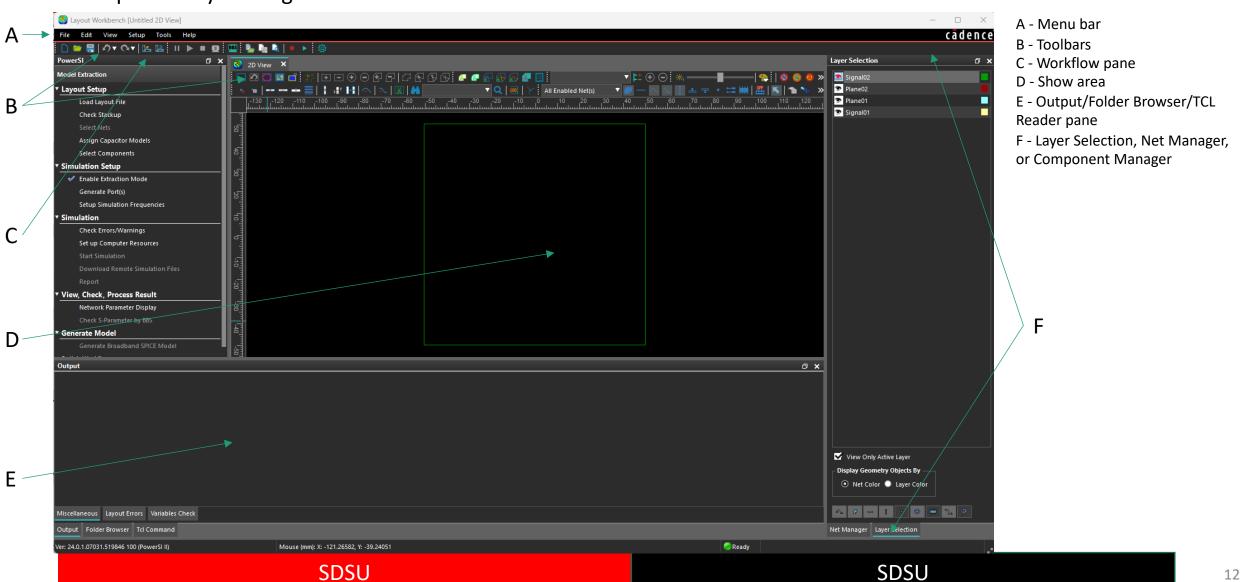




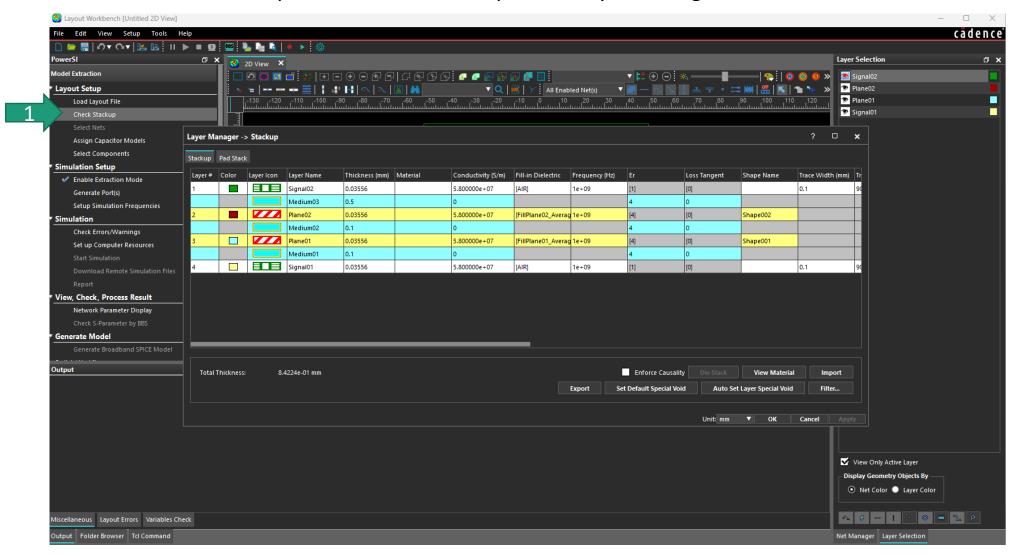
- 1. Click on File Menu
- 2. Click on New start a new project



- Major parts of the workplace when you open a new file in PowerSI.
- A square 4 layer design is created



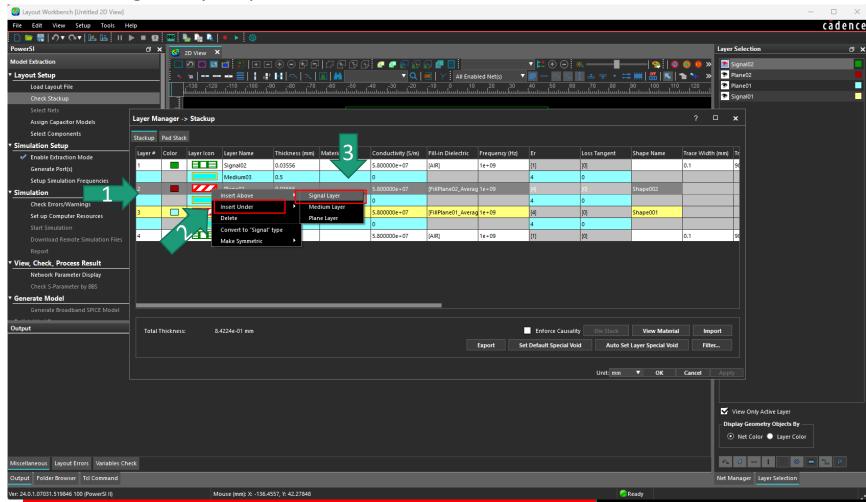
1. Select Check Stack up in the Workflow to open the Layer Manager



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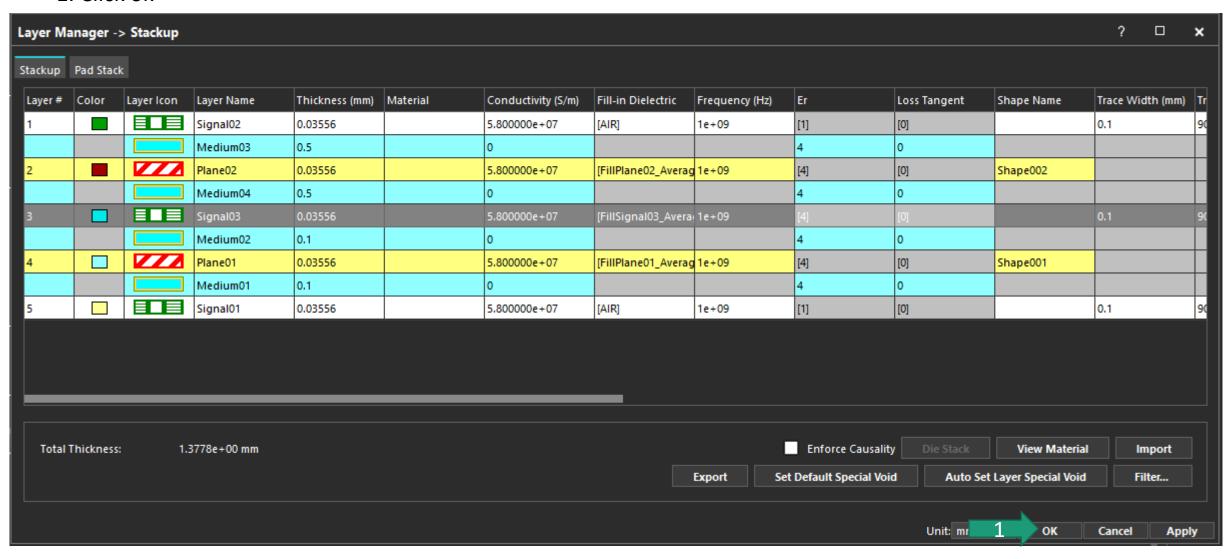
We will create a signal layer to create striplines (for another project)

- 1. Right click on layer 2 and
- 2. Insert Under then
- 3. Select Signal Layer option



This is our new 5 layer stackup

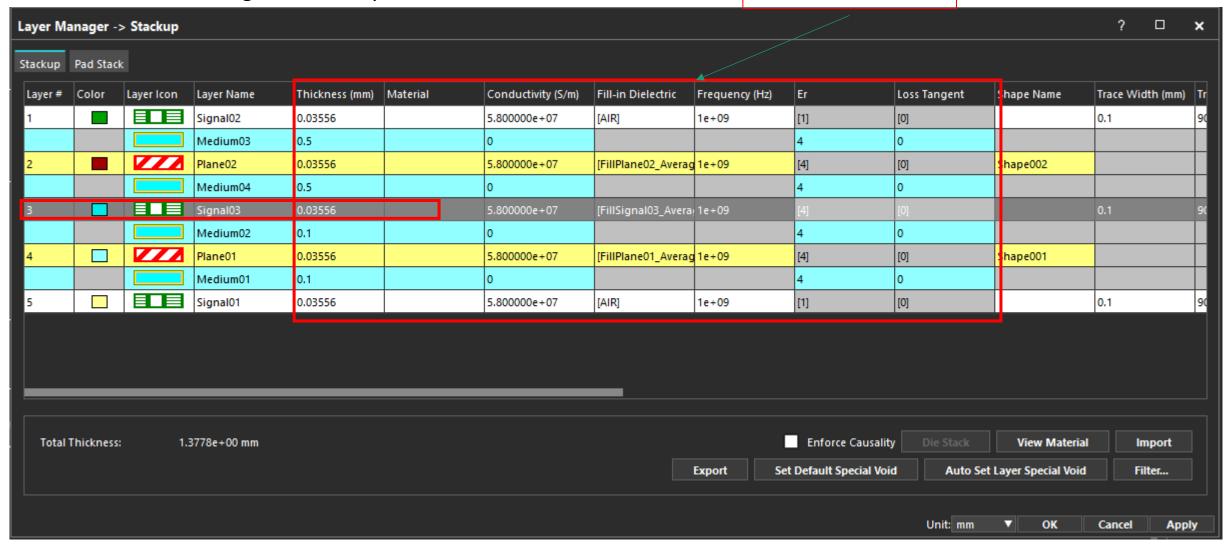
1. Click ok



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- This is our new 5 layer stackup
- Note surrounding dielectric layers

Editable fields

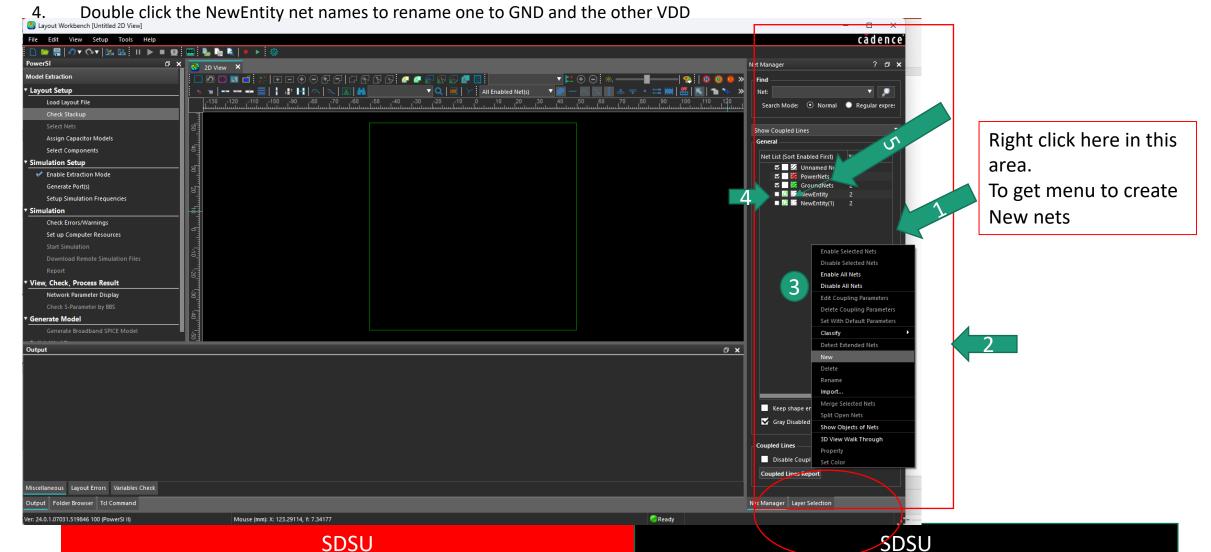


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#### Create two nets, VDD and GND

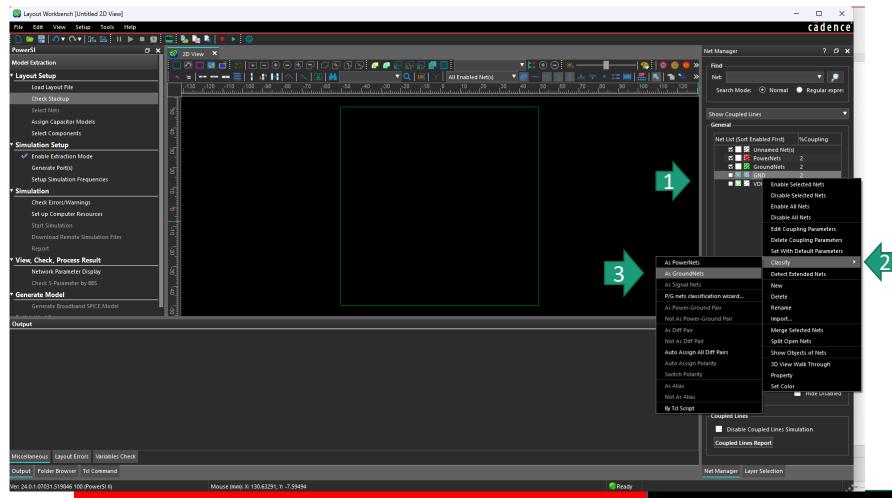
- 1. Right click in the Net Manager window
- Click New
- 3. Repeat steps 1 and 2

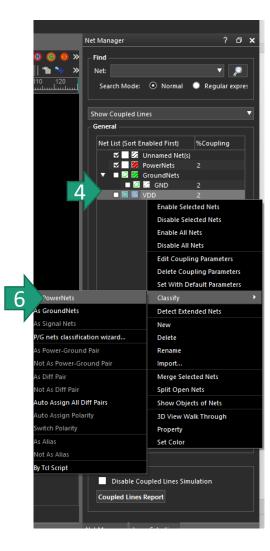
- 5. Click on box icon next to net name and Select green for GND color
- Select Yellow for VDD



Classify GND net as a GroundNet and Classify VDD as a PowerNet

- 1. Right click on GND net
- 2. Select Classify
- 3. Select As GroundNets
- 4. Right click on VDD net
- 5. Select Classify
- 6. Select As PowerNets



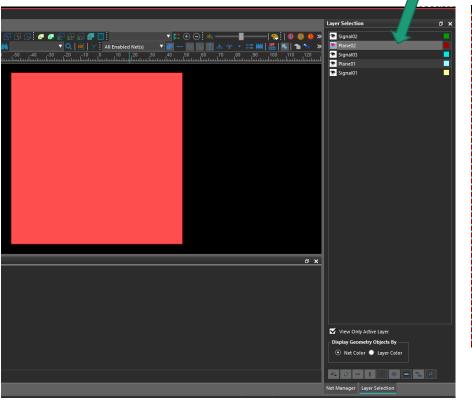


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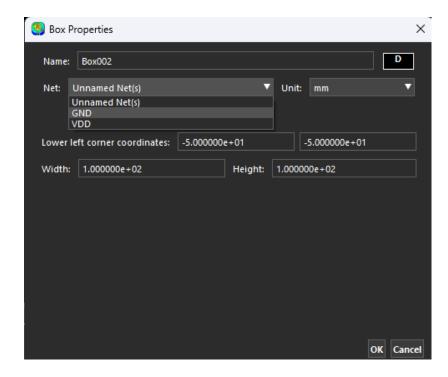
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#### Assign Plane02 to GND net

- 1. Select Plane02 as your active layer
- 2. Right Click on shape to get shape menu
- 3. Click on shape name Box002 to get properties
- 4. Assign shape to net GND from the pulldown menu

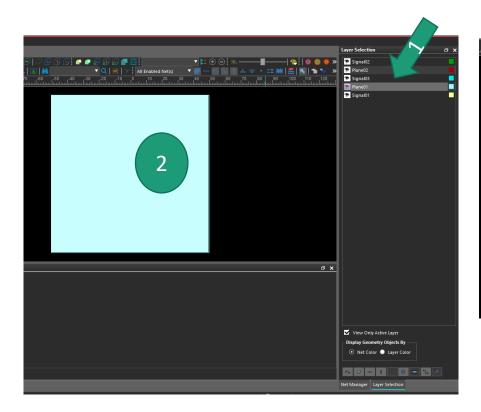


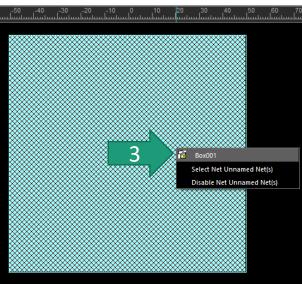


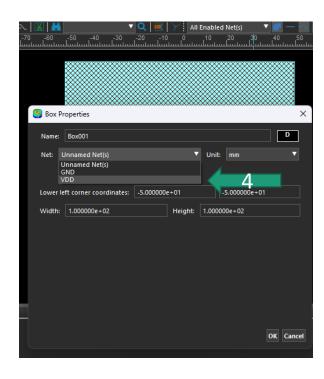


#### Assign Plane01 to VDD net

- 1. Select Plane01 as your active layer
- 2. Right Click on shape to get shape menu
- 3. Click on shape name Box001 to get properties
- 4. Assign shape to net VDD from the pulldown menu



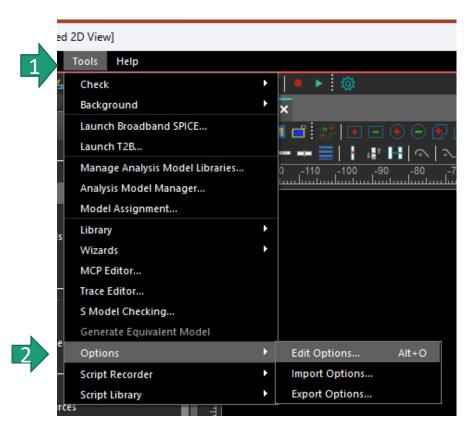


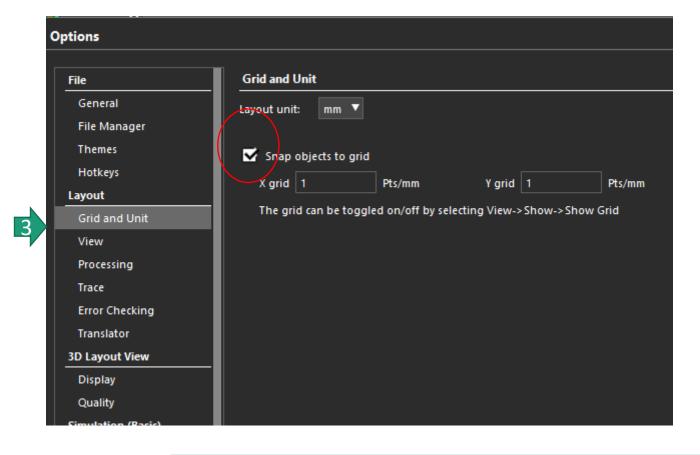


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#### Check grid settings

- Go to Tools menu
- 2. Select Options>Edit options
- In Options menu select Grid and Unit under Layout and set layout unit to mm and snap objects to grid



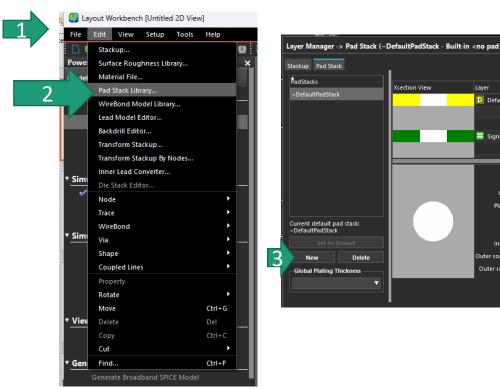


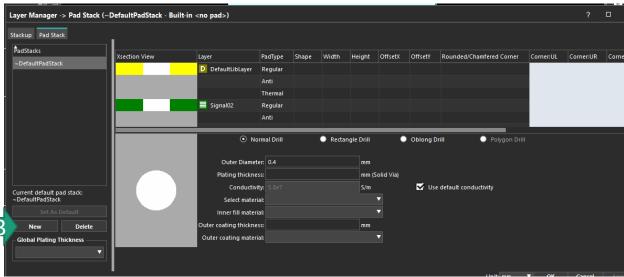
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#### Create a new padstack for model vias

Select the

- 1. Click on Edit menu and
- 2. select Pad Stack Library ...
- Click on New button to create new Pad Stack
- 4. Double click on NewPadStack and Rename to trainingPad

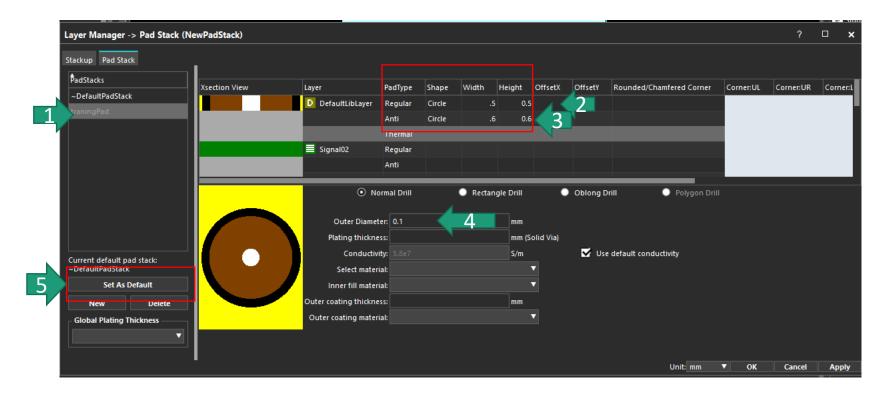




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Enter pad dimensions for DefaultLibLayer for new pad stack trainingPad

- Select the new pad stack trainingPad
- 2. Select circle for Pad Shape with width 0.5 mm for the DefaultLibLayer
- Select circle for Anti Pad with width 0.6 mm for the DefaultLibLayer
- Enter 0.4 for Outer Diameter
- 5. Click Set As Default button to set this via padstack as default for all vias



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#### Create vias for VDD and GND connections from SignalO2 Layer

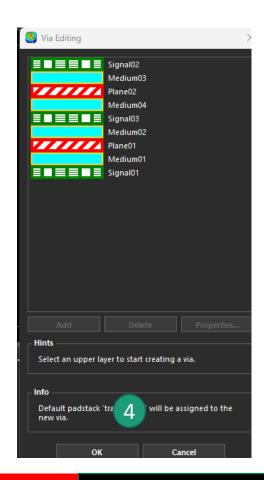
- 1. Left click on add via icon then left click on PCB area.
- 2. In the Via Editing window select upper layer to start creating via
- 3. Select lower layer to complete creating via.
- 4. The via will be created using the Default padstack
- 5. Click Add
- 6. Add vias using table below

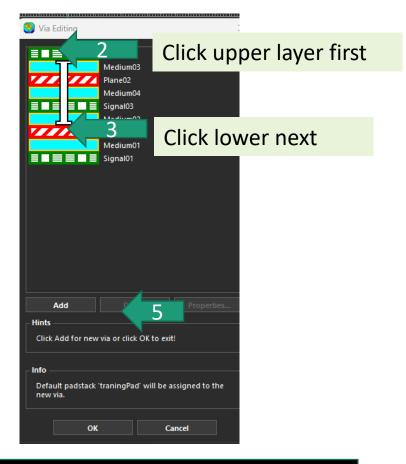


Via	X coordinate	Y coordinate	Layer connection
VDD	-35	12	Signal02 to Plane01(VDD)
VDD	-47.5	1.5	Signal02 to Plane01(VDD)
VDD	-25 6	-15	Signal02 to Plane01(VDD)
GND	-35	8	Signal02 to Plane21(GND)
GND	-47.5	-2.5	Signal02 to Plane21(GND)
GND	-25	-25	Signal02 to Plane21(GND)

#### Note:

- VDD vias will be from Signal02 to Plane01
- GND vias will be from Signal02 to Plane02

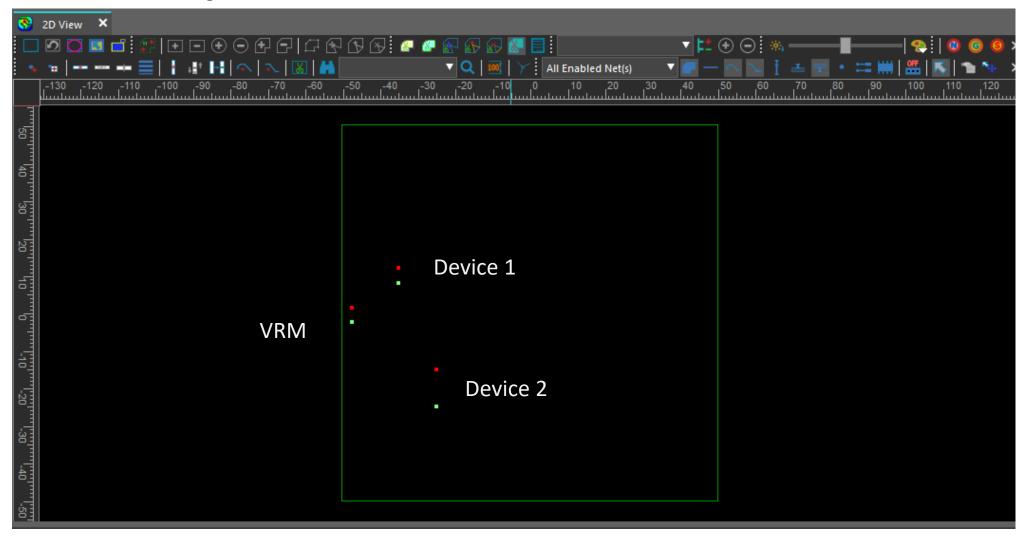




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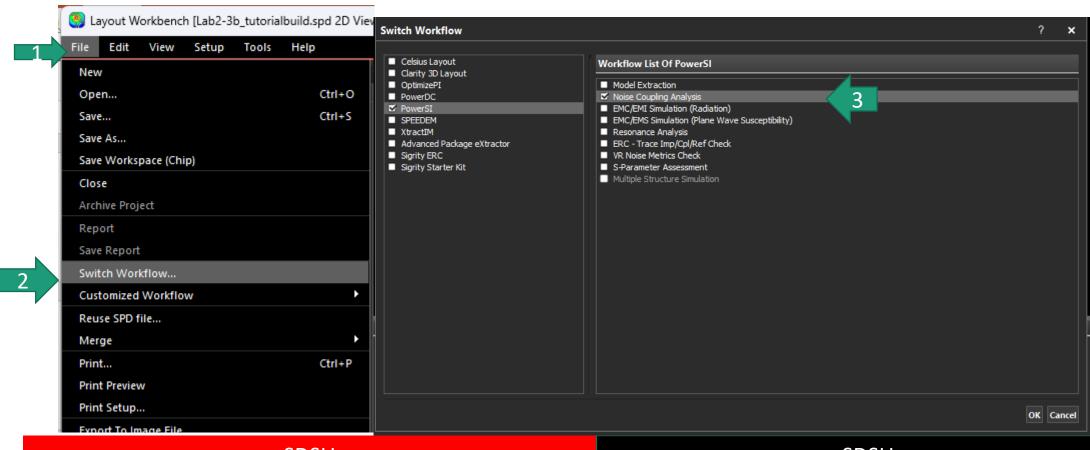
# IV. Setup a 5 layer PCB model in PowerSI-Step 7 PCB should look like image below after via placement

- Note the via labeling for devices and VRM



**SDSU SDSU** 

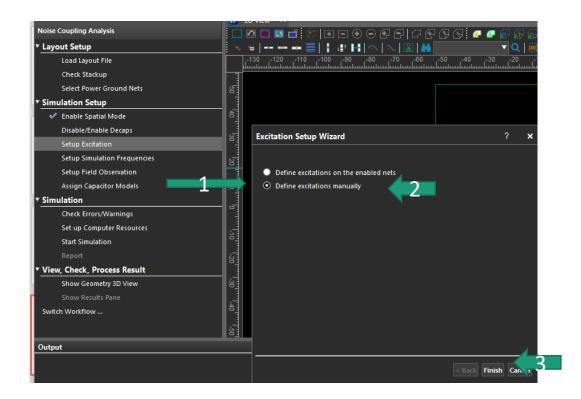
- 1. Click on File
- 2. Click on Switch Workflow
- 3. Select Noise Coupling analysis



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Add two excitation sources to layout to represent the active components in the design Steps:

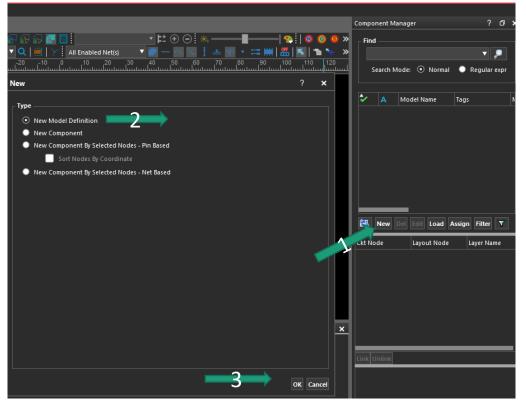
- 1. Click Setup Excitation
- 2. Click on Define excitations manually then
- 3. Click on Finish

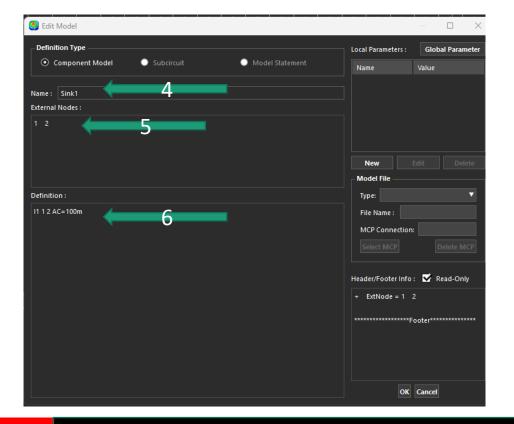


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#### **Define first model Sink1:**

- 1. Click New button in the Component Manager to select New Model Definition
- 2. Select New Model Definition
- 3. Click ok
- Name New Model Sink1
- 5. Provide two external nodes 1 and 2
- 6. Define an AC source of 100 mA

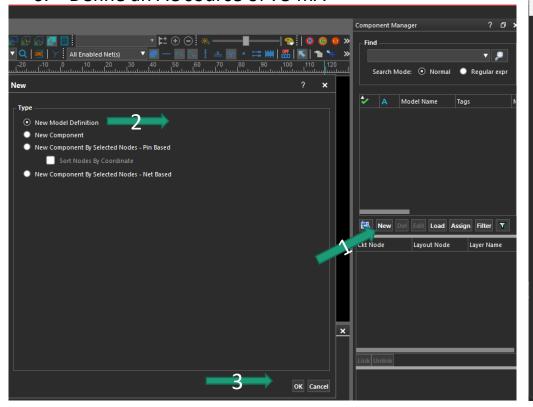


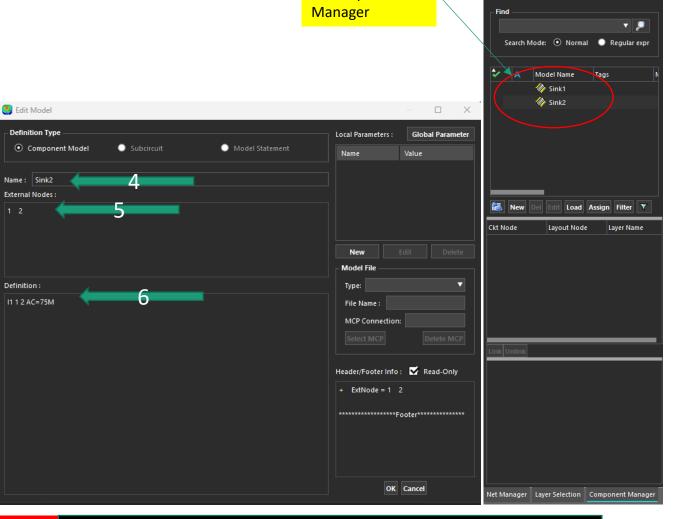


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#### **Define second model Sink2:**

- 1. Click New button in the Component Manager
- Select New Model Definition
- 3. Click ok
- Name New Model Sink2
- Provide two nodes 1 and 2
- 6. Define an AC source of 75 mA





Note two models

omponent Manager

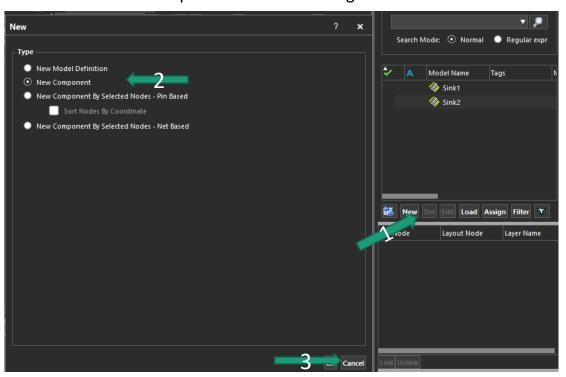
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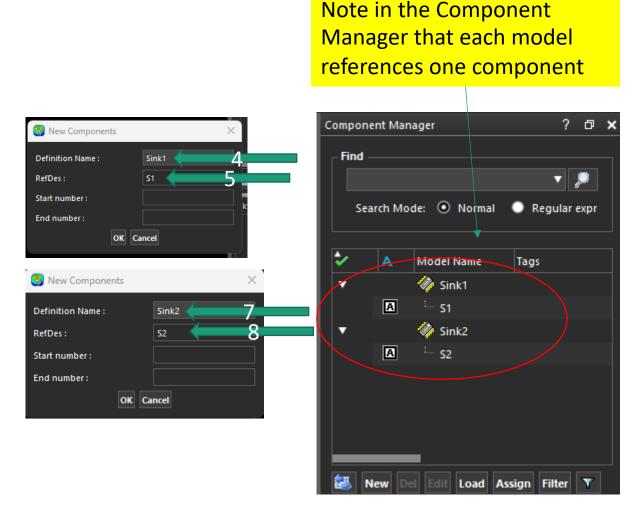
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in Component

#### Create two components that are referenced by models Sink1 and Sink2

- Click New button in the Component Manager
- 2. Select New Component Definition then
- 3. Click OK
- 4. Select Sink1 for the model Definition Name
- 5. Give component reference designator of S1 and click ok button
- 6. Repeat steps 1-3
- Select Sink2 for the model Definition Name
- 8. Give second component reference designator S2 and slick ok button

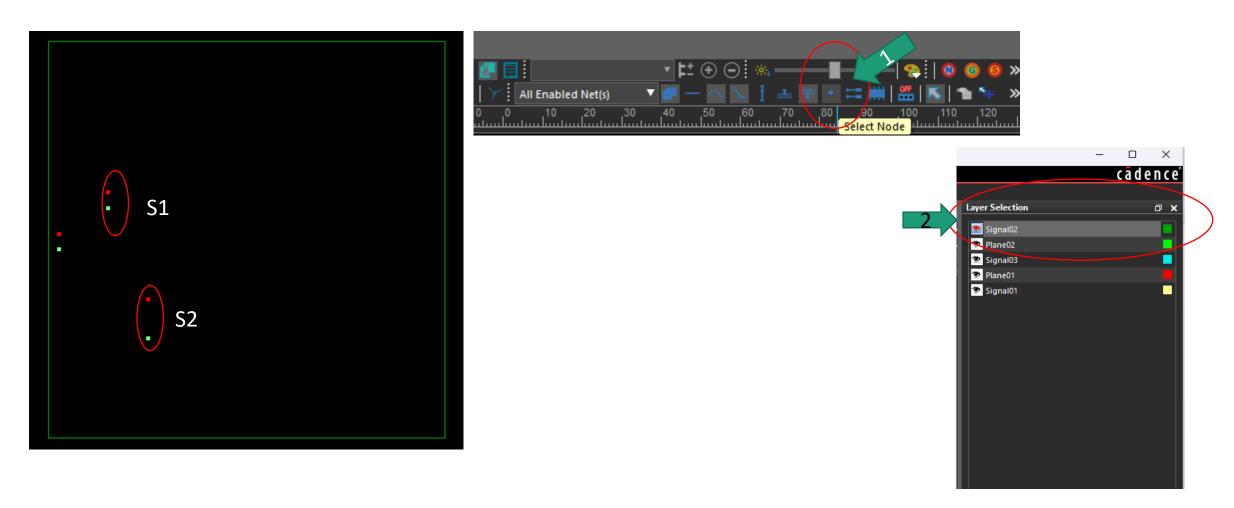




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Connect the two components to the layout VDD and GND nodes at locations shown below

- 1. Click on Node icon to activate to make sure we can select nodes in our layout
- 2. In Layer Selection Menu, Select Top Layer Signal 2 as the Active Layer

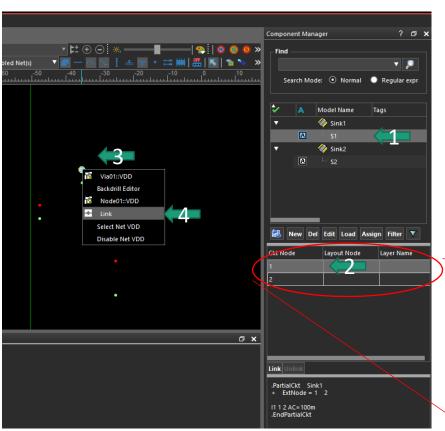


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#### Connect the two components to the layout VDD and GND nodes at locations shown below

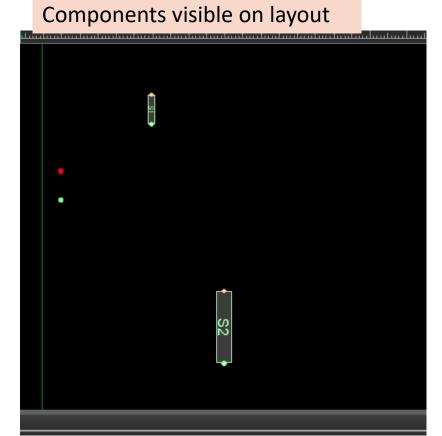
- 1. Left click on component S1 in the Component Manager
- 2. Left click on the S1 Ckt Node 1
- 3. Right click on VDD via node
- 4. Left click Link

- 5. Left click on S1 Ckt Node 26. Right click on GND via node
- 7. Left click link
- 8. Repeat steps 2-7 for component S2
- 9. Click on View>Show>Components to see components





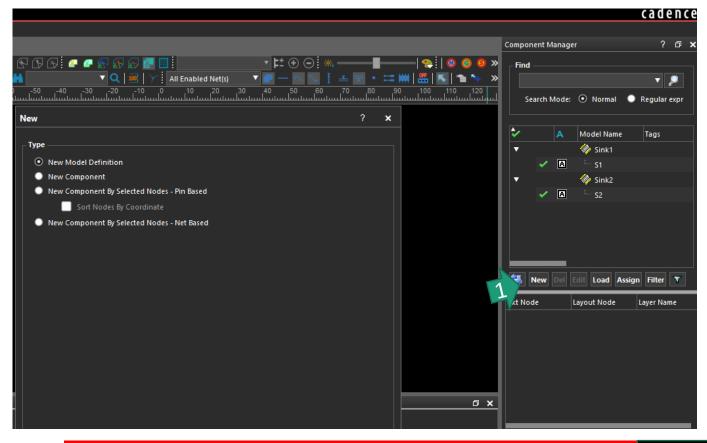
# After linking Ckt Node Layout Node Layer Name 1 Node01::VDD Signal02 2 Node07::GND Signal02

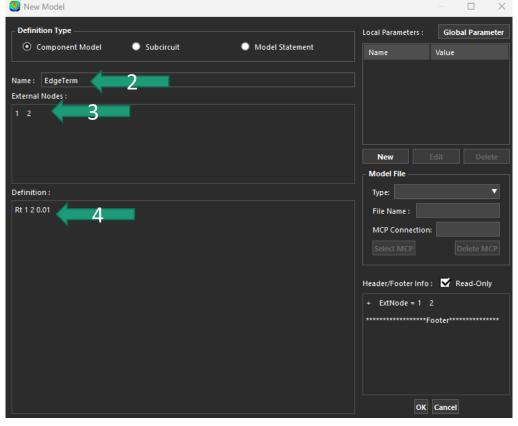


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Creating VRM terminating model as a resistor of .01 ohm

- Click new then New Model Definition
- 2. Name component model EdgeTerm
- 3. Add external nodes (12)
- 4. Define model as resistor with value 0.01 ohm





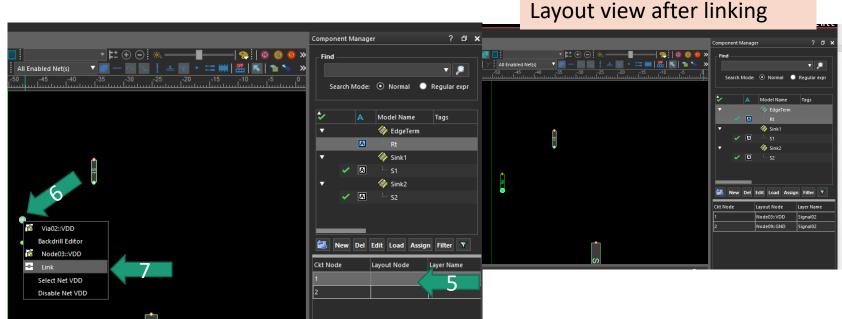
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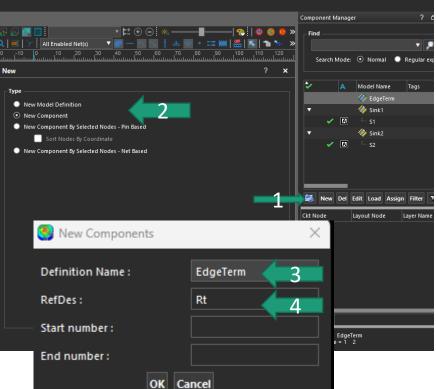
Creating a component using Edgeterm model and link to layout

- 1. Click New button
- 2. Select New Component Type (then click ok)
- 3. Select Name EdgeTerm
- 4. Give component reference designator of Rt then click ok)

- 5. Click Ckt Node 1 of Rt
- 6. Right click VDD node
- 7. Select link
- 8. Similarly click Ckt Node 2 of Rt
- 9. Select link

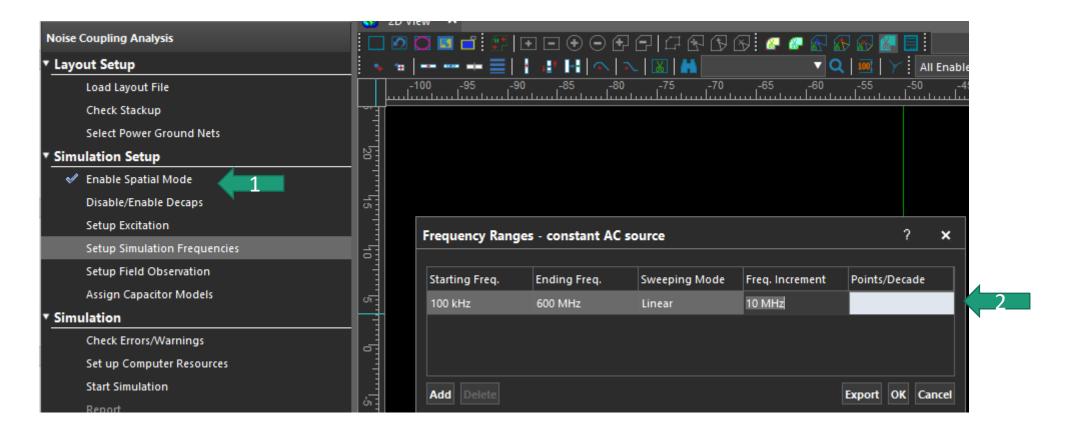
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#### **Setup Simulation Frequencies**

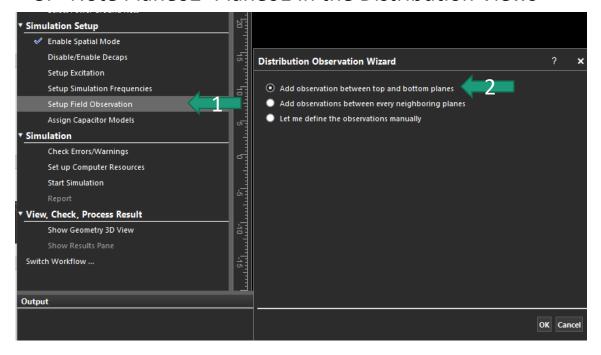
- Click on Setup Simulation Frequency to open Frequency Ranges for constant AC course\
- 2. Enter start, end and increment frequencies as in screen capture below

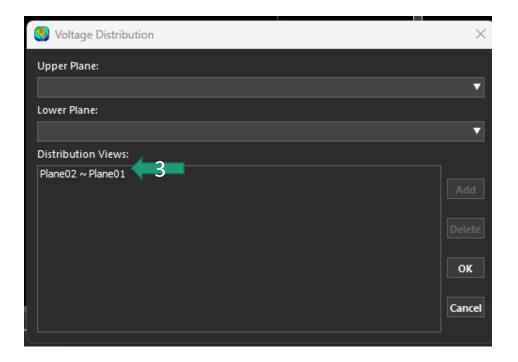


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Specify the plane layers to observe the voltage distributions

- 1. Click on Setup Field Observations
- 2. Select Add observation between top and bottom planes in the Distribution Observation Wizard
- Note Plane02~Plane01 in the Distribution Views



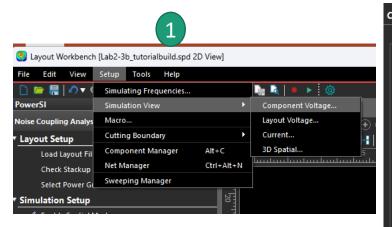


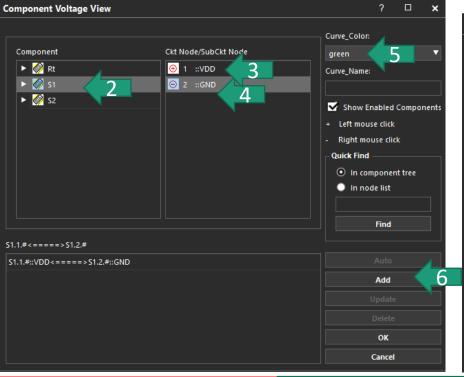
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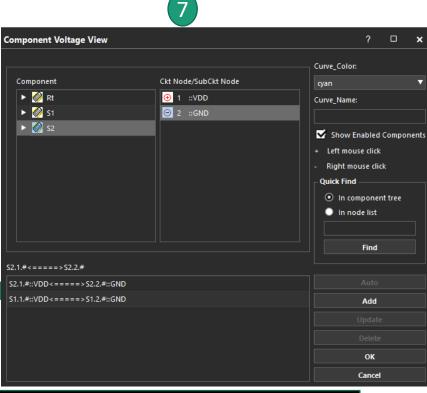
# IV. Setup for simulating with Spatial Workflow

#### Setup observation of voltages at components S1 and S1

- 1. Click on Setup>Simulation View>Component Voltage
- 2. Click on S1 Component
- 3. Left mouse click on Ckt Node 1 for positive node of observation point
- 4. Right mouse click Ckt Node 2 for negative node of observation point
- 5. Select green for the Curve Color
- Click Add button
- 7. Repeat steps 2-6 for S2 component, select Cyan for Curve Color



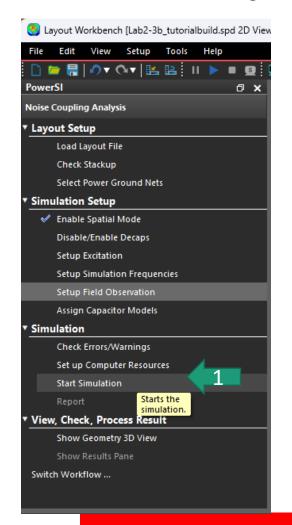


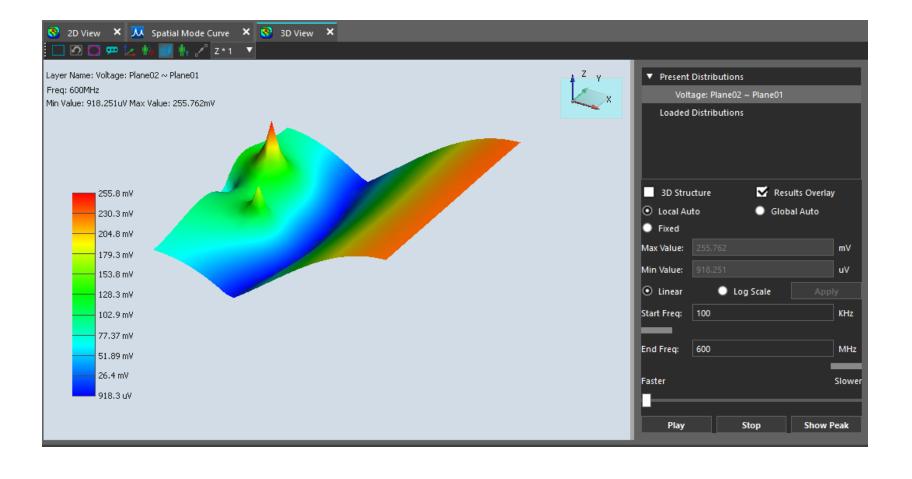


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#### Start the simulation

- 1. Click on Start Simulation in the workflow panel
- 2. Note that voltage distribution simulates across the frequency bandwidth we setup and stops at end frequency (600MHz)

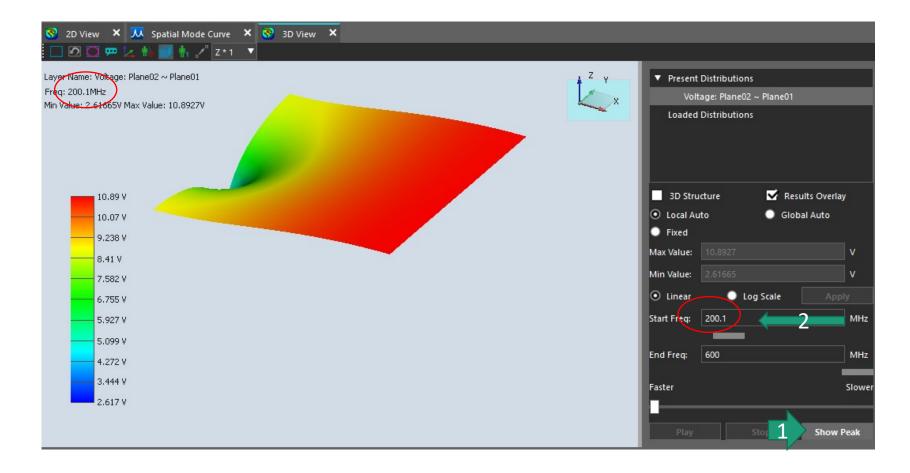




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Find the peak voltage level and frequency at which it occurs

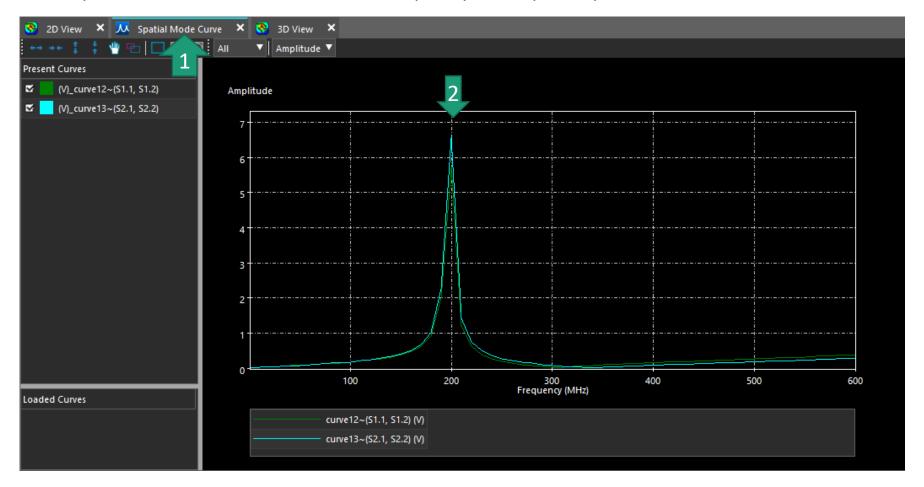
- 1. Click Show Peak button to see maximum distribution voltage is about 8.4 V
- 2. Slide the frequency slider to find peak frequency at about 200 MHz



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# V. Running Spatial mode simulation Find the peak voltage level and frequency at which it occurs from Spatial Mode Curve

- Click the Spatial Mode Curve to see voltage distribution are our two observation points
- Note peaks at 200 MHz due to resonant frequency of the power planes

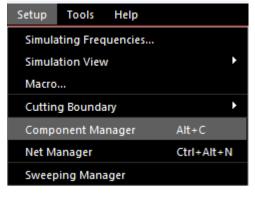


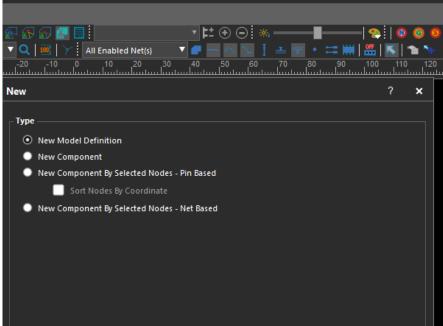
**SDSU SDSU** 

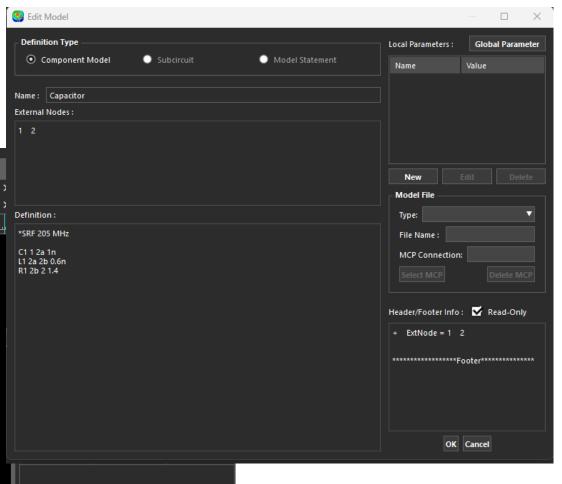
Add decoupling capacitors to reduce the peak voltages at the sink locations and across the layout

First Create new model definition for decoupling capacitors

- 1. Click Setup>Component Manager>New button
- 2. Select New Model Definition
- 3. Name model Capacitor
- 4. Provide External Nodes
- 5. Define a capacitor with self resonance model of 205





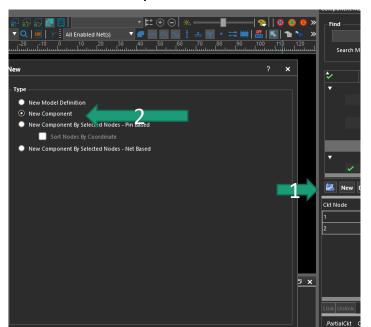


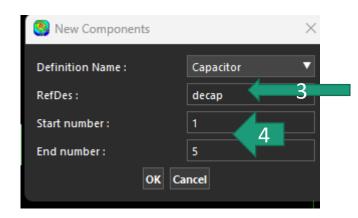
**SDSU** 

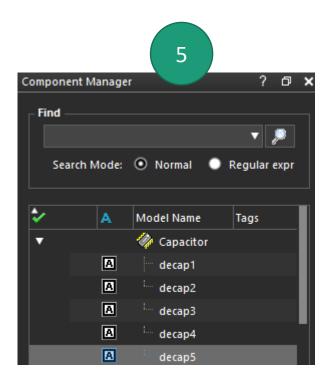
Add decoupling capacitors to reduce the peak voltages at the sink locations and across the layout

Create 5 decoupling capacitors form Capacitor model

- 1. Click New button in Component Manager
- 2. Select New component
- 3. Give Reference designator name 'decap'
- 4. Enter 1 for start number and 5 for end
- 5. Note 5 decap references are create for Capacitor model



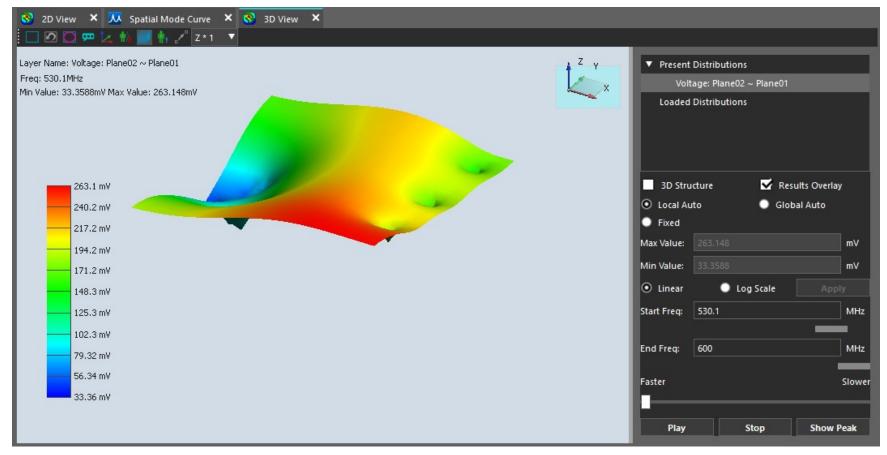




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Add decoupling capacitors to reduce the peak voltages at the sink locations and across the layout

- Create VDD/GND vias next to sinks and in the voltage 'hotspots'
- 2. Connect decaps at these locations
- 3. Rerun simulation to see reduction in peak voltage distribution
- Note reduction to 263.1mV



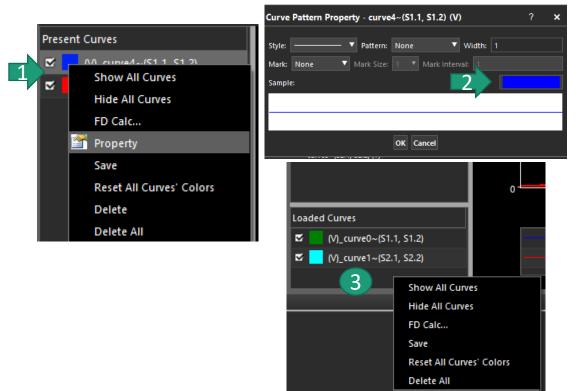
SDSU

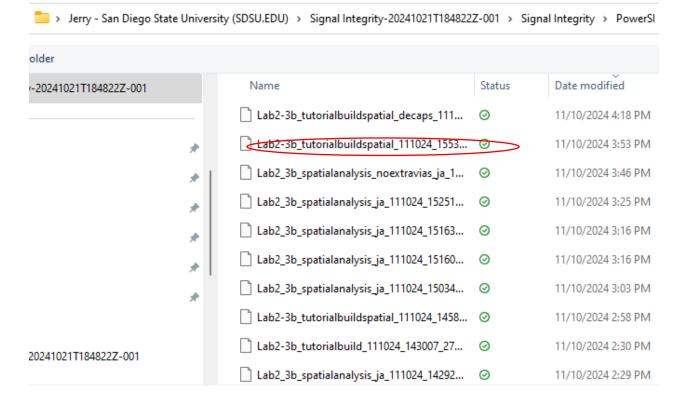
Add decoupling capacitors to reduce the peak voltages at the sink locations and across the layout

Change colors of peak voltages (right click color box next to curve name)

Load

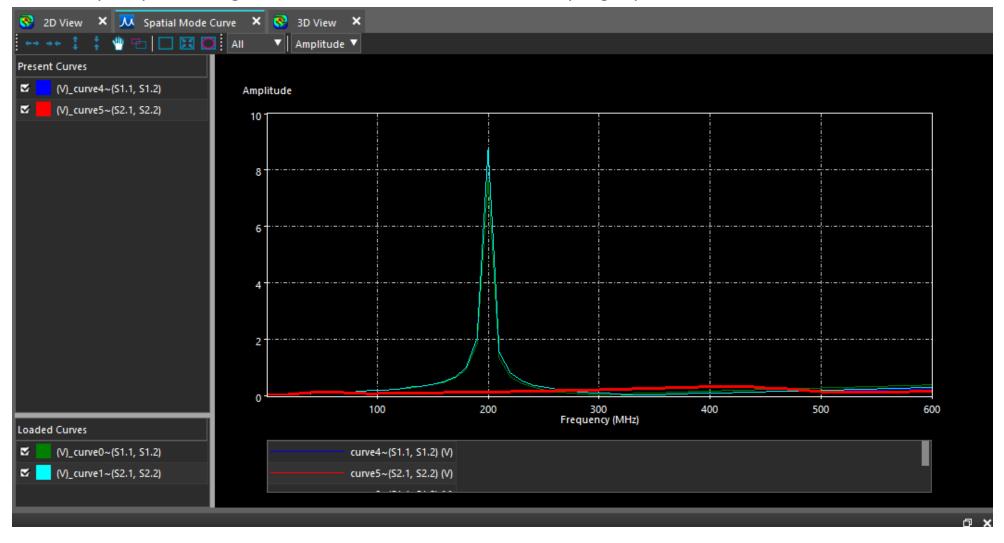
- Select preferred color
- Load Curves from simulation with no decaps by Right click in Loaded Curves area and selecting appropriate file from automatically saved files for each simulation





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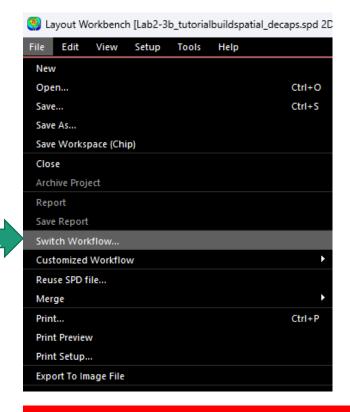
# V. Running Spatial mode simulation Compare peak voltage distribution with and without decoupling capacitors

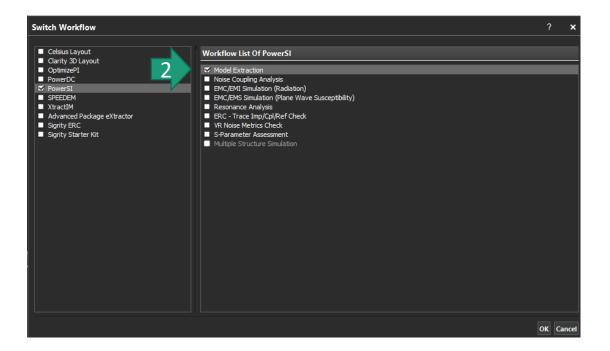


**SDSU SDSU** 

In the current model using spatial mode simulation:

- 1. Change to Workflow to Model Extraction
- 2. Save with new model name e.g.<original name>\_extractionversion

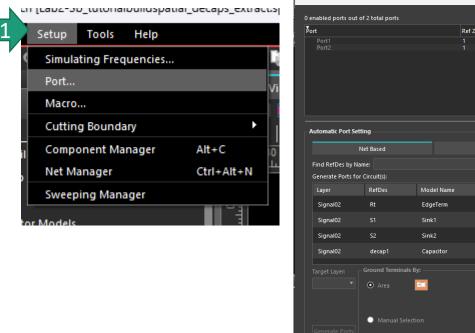


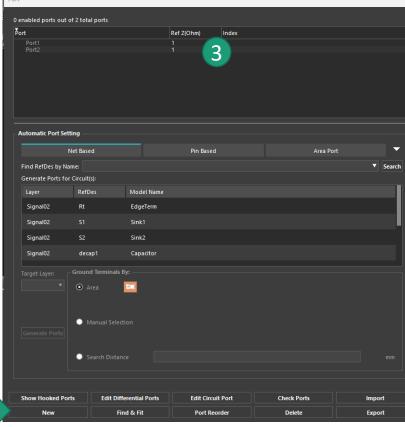


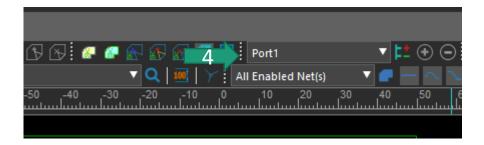
SDSU

Use Ports for Extraction Workflow

- 1. Go to Setup>Port...
- 2. Click New button twice
- 3. Change Reference Z(ohm) to 1 ohm (then close Port menu)
- 4. Select Port1 in the menu bar pulldown menu

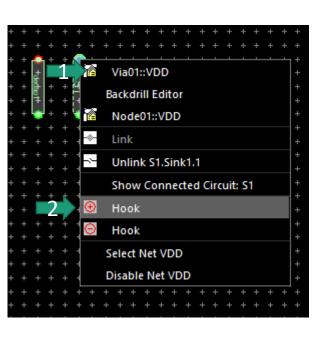


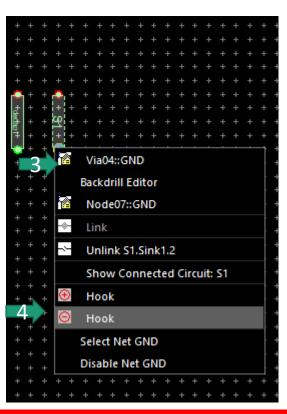




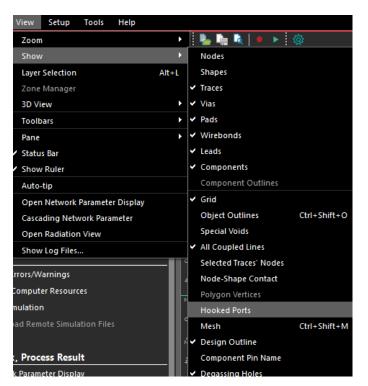
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- 1. Right click on VDD via originally connected to S1
- 2. Select positive Hook to connect positive port terminal to VDD
- 3. Right click on GND via orginally connected to S1
- 4. Select negative Hook to connect negative port terminal to GND
- 5. Show ports View>Show>Hooked Ports
- 6. Similiary repeat steps for S2 location

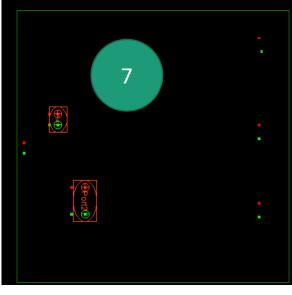








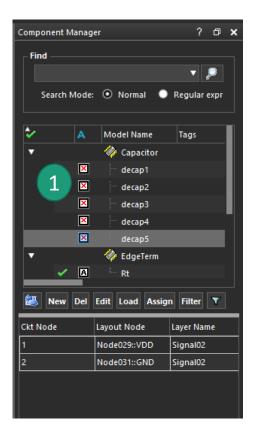
#### 7 View>Show>Hooked Ports

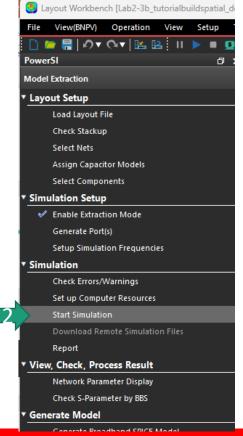


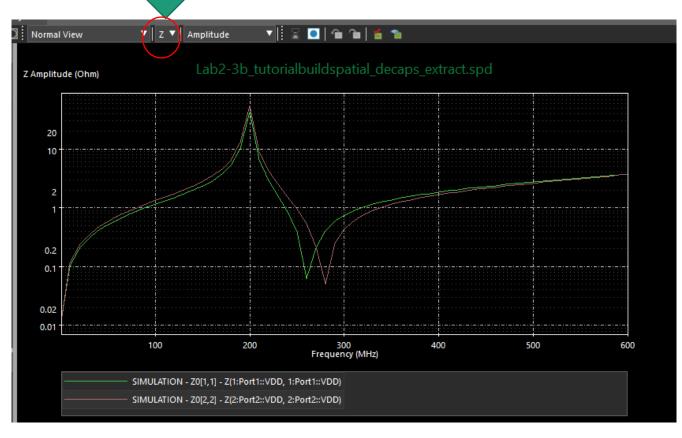
1. Go to Component Manager and deactive decaps in your model before extraction simulation (click A box twice to see a red X to indicate component is deactivated)

2. Start Simulation

3. Select Z parameters from the Extraction menu options

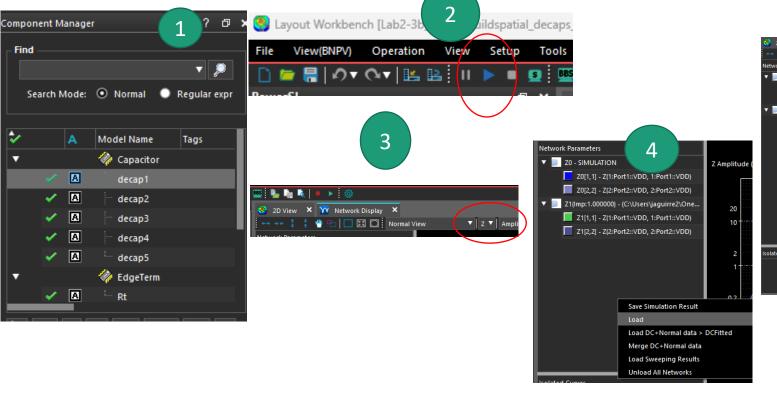


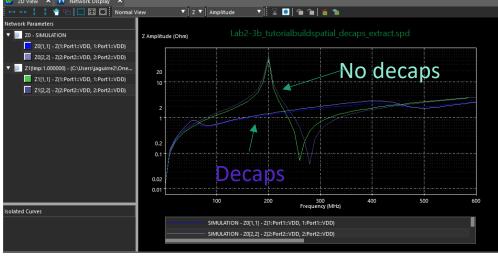




- 1. Go to Component Manager and reactivate decaps in your model before extraction simulation (click A box once)
- 2. Go to Tool bar and click Start Simulation blue arrow
- 3. Select Z parameters from the Extraction menu options

4. Right click in Network Parameters panel and load simulation without decaps for comparison





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# The End